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Solar Cell Performance after Exfoliation Using Sonic Liftoff

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Received: 21 January 2025 | **Revised:** 14 May 2025 | **Accepted:** 8 June 2025

Funding: US Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office, Grant/Award Number: 08973

Keywords: III–V | photovoltaics | spalling

ABSTRACT

Removing grown device layers from a GaAs substrate is an essential aspect of reducing costs of III–V photovoltaics. While many methods of device layer removal have been explored, Sonic Lift-off (SLO) demonstrates novel control of the stress conditions within the substrate during exfoliation. By utilizing acoustic energy, this technique allows for a lower maximum stress required to fully lift-off layers from a substrate. We demonstrate that this technique results in no damage to inverted-grown and upright-grown exfoliated devices. The inverted device demonstrated an efficiency of 26.8% after SLO in comparison to 26.5% for a traditionally-processed cell, and the upright device showed a 22.0% efficiency after SLO. The SLO process has been shown to produce exfoliated, damage-free devices and opens the door for substrate reuse to reduce the cost of III–V photovoltaics.

1 | Introduction

The path for improved photovoltaic (PV) devices has always been to reduce manufacturing cost by making cells thinner, more efficient, and longer-lasting. As the industry matures, cell costs are becoming dominated by those of materials, and process improvements are yielding small cost benefits. Next generation solar cells and modules capable of meeting the U.S. Department of Energy's 3 cents/kWh target will require fundamental scientific breakthroughs [1]. Today the highest-efficiency PVs are made of III–V material, and the market size for such devices is growing [2]. Despite this, the higher cost of III–Vs has confined their application to space power systems and more specialized applications [3]. The implementation of III–Vs in emerging markets such as unmanned aerial vehicles (UAV) and low-earth orbit satellites (LEO) has accepted cost structures of \$10–300/ W_{DC} [4]. However, large terrestrial deployments (e.g., vehicle-integrated PV or concentrated PVs) or portable integrated markets (e.g., the Internet of Things, IoT), that are expected to grow up to 10 GW/year, require cell manufacturing costs well below \$10/W_{DC} [5].

A key fraction of the cell manufacturing cost for these III–V cells is the substrate cost - not only its intrinsic market value but also its present lack of re-usability. To date the substrate cost sits at about \$20/W (>30% of total cost) for both single junction (1J) and two junction (2J) GaAs-based solar cells [4]. The high contributing factor of substrate cost makes techniques that can reuse a substrate attractive, of which the main industrial approach has been the use of epitaxial lift-off (ELO) [6, 7]. ELO separates a device layer from a GaAs substrate by using hydrofluoric acid (HF) to selectively and laterally etch a sacrificial layer (AlAs) grown between the device film and the GaAs substrate. This process requires an occasional use of high-cost chemo-mechanical polishing (CMP) to continually produce a substrate usable for high-quality growth [8, 9]. When substrate reuse is employed, the total substrate costs are driven by three primary factors: the substrate price, the number of reuses, and the cost of CMP and reclaim [8–10]. Eliminating the need for a costly CMP and reclaim due to the prolonged exposure to HF could lower the cost to below the $10 mark [11]. While other materials, such as Ge, can employ a porous layer to successfully remove device layers without harmful HF etching and potentially without CMP to reclaim the substrate, that technology does not exist for GaAs [12, 13].

An alternative substrate reuse method to ELO for GaAs is spalling - the lateral fracture of the GaAs substrate and removal of device layers with the intention of regrowing device layers on and respalling the GaAs substrate. This requires a stressor in tension that is well bonded to the layers being removed. In a GaAs spalling system, the nonpolar planes within the crystal preferentially spall, resulting in a faceted surface when spalling (100) GaAs substrates. In a spontaneous spalling system, where no energy is added to the system, the tension in the stressor must be high enough to propagate a spall across the the entirety of a wafer. This resulting residual stress due to the high tension in the stressor can cause cracking as the removed device layers are handled [14]. Controlled spalling inputs energy into the system as spalling occurs, allowing for reduced residual stress from the stressor layer after the spalling event. Some controlled spalling techniques are performed at room temperature, but require the application of a thick stressor layer (often nickel), that can be difficult to remove if desired and can put the exfoliated device layers under residual stress.

Sonic Liftoff (SLO) is a controlled spalling technique that has been developed by Crystal Sonic, Inc. Unlike other controlled spalling techniques, SLO utilizes a polymer stressor and a reduction in temperature of the system to increase the stress in the system via the mismatch in the coefficient of thermal expansion. This allows for a reduced stress on the device layers at room temperature, where most device processing is performed. The SLO process also utilizes ultrasonic waves as the supply of energy to propagate the spall across the energy of the wafer. The ability to input energy in this way can reduce the stress the device layers see during a spalling event, minimizing the chance of cracking in the device layers. In addition, with careful modulation of these ultrasonic waves, the faceting inherent to spalling a (100) GaAs substrate can be greatly reduced [15], potentially decreasing or eliminating the need for CMP between spalling events, providing increased cost reduction [11].

Here, we present a substrate reuse pathway employing an acoustic lift-off technique developed by Crystal Sonic Inc., namely, SLO. The process does not rely on metal deposition steps or damaging etchants, and controls the maximum stress required for complete device layer removal. We share SLO results on inverted- and upright-grown GaAs devices, grown at the National Renewable Energy Laboratory (NREL) and Rochester Institute of Technology (RIT) using metal-organic vapor phase epitaxy (MOVPE), showing no degradation between the control and the SLO solar cells.

2 | Experimental Section

2.1 | MOVPE Growth

Solar cells were grown by MOVPE. Inverted devices were grown at NREL in a custom-built atmospheric pressure reactor. The substrates were (100)-oriented GaAs, single-side polished and miscut 2° toward <111>B. The substrates were 350 µm thick and 2” in diameter. Precursors included trimethylgallium, trimethylindium and trimethylaluminum for the group-III elements; arsine and phosphine for the group-V elements; diethylzinc, carbon tetrachloride, disilane, dilute hydrogen selenide for the dopants; and dimethylhydrazine for nitrogen. Before growth, the substrate was etched in NH_4OH : H_2O_2: H_2O (2 : 1 : 10 by volume) for 2 min and then rinsed in deionized water and dried with nitrogen. The sample was loaded into the center of the reactor and heated to 650 °C under an overpressure of arsine mixed with purified hydrogen flowing at 6 lpm. After deoxidizing the surface at 650 °C for 10 min, a GaAs seed layer was grown, followed by the rear-heterojunction device layers shown in Figure 1. The

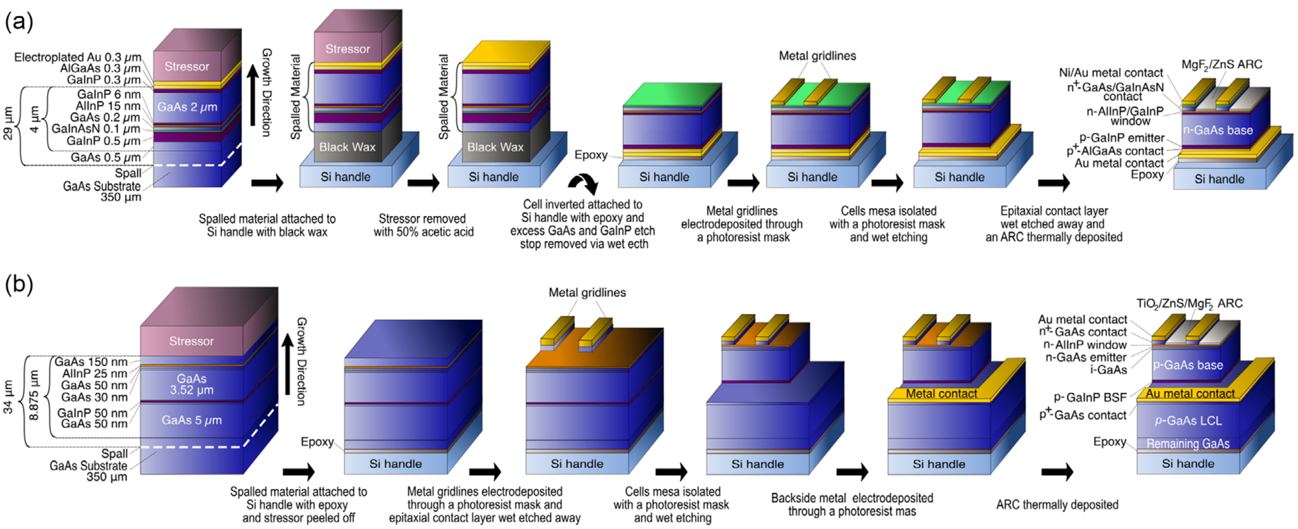

FIGURE 1 | Schematics of a) as-grown cell stack of inverted device and the process flow through of creating an inverted solar cell; b) as-grown cell stack of upright device and the process flow through of creating an inverted solar cell (not to scale).

structure was grown at 650 °C, except for the GaInAsN front contact layer at 570 °C and the AlGaAs back contact layer at 620 °C. Growth rates ranged from 2 to 6 μm/min and V/III ratio ranged from 10 to 200. At the end of the growth, the sample was cooled to room temperature under an arsine overpressure.

Upright front homojunction devices were grown at RIT in an AIXTRON 3x2" close-coupled showerhead, low-pressure MOVPE reactor. Group III precursors were trimethylgallium, trimethylindium, and trimethylaluminium. Group V sources were arsine and phosphine. Dopant sources were disilane, diethyltellerium, diethylzinc, and carbon tetrachloride. In situ telemetry was recorded using a LayTec EpiCurveTT system, which provides film growth rates, substrate surface temperature by emissivity-corrected pyrometry, and wafer curvature using a split-beam laser. Reactor pressure was maintained at 100 mBar during growth. Following a 10 min bake at 700 °C under arsine to desorb oxides, growth temperatures ranged from 575 to 650 °C and V/III ratio in the absorber layer was 45. Each device was grown on an full 50.4 mm diameter, epi-ready, commercial wafer. A 5 μm thick, 1E20 $cm-^{3}$highly doped GaAs lateral conduction layer was deposited prior to the device layers in order to implement a top–top contacting scheme, as well as serve as a buffer over the spalled surface in future device growths.

2.2 | SLO

After growth of the device structures, a gold back contact was electroplated to the back contact layer for the inverted device grown at NREL. The upright device grown at RIT did not have metallization prior to SLO. Both samples then went through the SLO process, consisting of four steps: 1) forming a crack notch on the substrate's edge, that serves as the point of crack initiation; 2) bonding of the substrate to a stressor layer made of a removable polymer; 3) cooling of the sample between −60 and −100 °C through an INSTEC-HCC214S cold plate; and 4) applying acoustic waves into the sample. Under these conditions, the difference in the coefficient of thermal expansion (CTE) between the substrate and stressor layer, combined with the acoustic waves lead to the lateral propagation of a crack along the spalling plane all across the diameter sample [15, 16].

Independently investigating the effect of device performance, the SLO process has been studied for spall depth and effect of ultrasonic modulation. A spall depth of 15, 20, 25, 30, and 35 μm was targeted by varying stressor thickness over a total of 100 GaAs wafers without growth. The spall depth was measured by a cross-sectional scanning electron microscopy (SEM) of the exfoliated film and an average calculated. In addition, three different ultrasonic modulations were also studied. The modulations targeted there different crack speeds, measured by an In-plane Crack Dynamics technique as described in ref. [17]. The surface analysis of the spalled wafers was performed with a Bruker DektakXT stylus profilometer (2 μm-radius tip) and linearly graphed from the flat (spall initiation) to the opposite side of the wafer. Surface profile maps of the spalled surfaces were generated with Vision64 Map software (Bruker Corp).

2.3 | Device Processing

After spalling, the exfoliated semiconductor layers were processed in a photolithography cleanroom into functioning solar cells. The inverted sample was secured temporarily to a silicon handle with black wax and the semiconductor layers were detached from the stressor in a mildly acidic solution (50% acetic acid) for 30 min. The sample was bonded to a permanent silicon handle with low viscosity epoxy (Henkel Loctite Eccobond 931-1) and detached from the black wax. The GaAs and GaInP sacrificial layers were then etched away; front grids were electroplated through a Shipley S1818 photoresist mask; individual 0.115 cm^2 cells were isolated by wet-chemical etching. Finally, a bilayer MgF_2/ZnS antireflection coating was deposited by thermal evaporation. Baseline inverted cells were processed starting with the electroplating of the gold back contact and bonding to a permanent silicon handle. The substrate was then etched away in $NH_4OH : H_2O_2(1:3)$. The remainder of the processing followed the procedure for the spalled cells.

Following growth of upright devices, one device wafer was retained as an on-substrate control while the other wafer had its device layers spalled using the SLO process. The spalled device layers were epoxied to a blank Si wafer as a permanent carrier. Solar cell fabrication then proceeded using standard III–V techniques, including contact photolithography, wet chemical etching, and electroplating to define a variety of cell sizes on the same mask set. The upright-grown data presented here were measured on 2.5 by 2.5 mm devices. The top contact grids were defined using AZ 1512 positive broadband photoresist and electroplated using Transene TG-250 gold sulfite solution. In order to avoid compromising the bottom lateral conduction layer during a later step, the n-type GaAs top contact layers were etched prior to mesa isolation using a 2:1:50 mixture of NH_4OH:H_2O_2:H_2O. Next, device mesas were defined and isolated by etching the III-P layers in 1:1 HCl:H_3PO_4 and etching the III-As layers in 3:4:1 H_3PO_4:H_2O_2:H_2O. Finally, the bottom common contact to the lateral conduction layer was defined and electroplated similarly to the top contact grids. Following initial electrical testing and characterization, an antireflection coating was deposited by thermal evaporation targeting 10 nm TiO_2, 50 nm ZnS, and 90 nm MgF_2. No additional encapsulation was used.

2.4 | PV Characterization

Inverted solar cells were measured at NREL using standard PV techniques. External quantum efficiency (EQE) was measured on a custom-built instrument with a tungsten-halogen lamp and a 270 m monochromator. Current–voltage (IV) curves were measured on a custom-build solar simulator using a xenon white light source and a calibrated GaAs reference cell, with the intensity adjusted to simulate the AM1.5G G173 solar spectrum at 1000 W/m^2 [18].

Upright devices were characterized at RIT under simulated 1-sun AM1.5G conditions using a TS Space Systems dual-source close-match solar simulator [19] calibrated with reference InGaP and GaAs single junction cells certified by NREL. Spectral response was measured using a Newport IQE-200 system.

3 | Results

3.1 | SLO

The high surface faceting of GaAs during spontaneous spalling is due to the high stress input to the system stress needed to fully propagate a crack through a substrate. As the stress field around the crack tip (also known as the stress intensity factor, K) exceeds the critical stress for the material (K_{IC}), a crack forms and propagates until the K-value decreases below K_{IC}, where the crack arrests [20, 21]. In a spontaneous spalling system such as that described by Farah [22], the stress required for spalling is caused only by the coefficient of thermal expansion difference in the stressor and the substrate as the system is cooled. This is referred to as the thermal load of the system. In the case of spontaneous spalling, the minimum stress (K_{Imin}) necessary to fully propagate a crack across a wafer needs to be much higher than the critical stress as shown in Figure 2a. Without a high K_{Imin}, the characteristic deceleration of the crack will stop the crack front inside the material [20, 21]. This results in exfoliated device layers that are inherently under a great amount of stress until stabilized by attaching to an external handle or removal of the stressor layer.

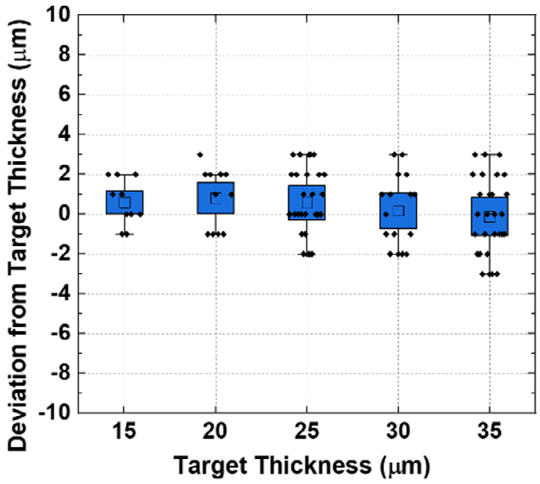

FIGURE 3 | The deviation from a target thickness for different spall depths. The blue box shows the standard deviation of the points, the whiskers show the 10th and 90th percentile, and the open box shows the average value.

In contrast, the SLO technique presented in this work offers much greater control over the stress conditions within the substrate. By prestressing the sample to just below K_{IC}, a weak plane is created at the desired cleaving depth. The amount of prestress the system undergoes, and therefore the cleaving depth, is determined by the thickness of the stressor applied, with a thinner stressor applying less stress. Out of 100 spalled 2" GaAs wafers, five spall depths were targeted and the spalled pieces evaluated for their average thickness (Figure 3). The shallower the target spall depth, the less variation of thickness is observed, but the average thickness deviates slightly more than desired. The variations introduced during certain steps of the SLO process (e.g., stressor application) are proportional to the target thickness. Therefore, at lower target thickness the variation decreases as well. This likely can be adjusted as more data on stressor thickness in relation to spall depth becomes available. By having an adjustable spall depth that is easily controlled by stressor thickness, the SLO process is tunable to accommodate multiple device structures. Given a minimum handling thickness of 150 μm for the substrate and a spalling thickness of 16 μm (the lowest presented here), a 350 μm substrate has a maximum reuse potential of 12 times if no material must be removed between spalling events to reclaim a wafer. A 500 μm substrate could be reused up to 21 times.

While the spall depth is controlled by the stressor thickness, the crack propagation is then controlled by altering stress conditions around the crack tip using acoustic waves, as shown in Figure 2b. In the SLO process, an acoustic transducer is coupled to the system and the acoustic waves impart enough energy to move the crack front through the substrate independently of the thermal stress [16]. This allows for a stressor layer that imparts an 15–25% less stress on the exfoliated layers, as the maximum

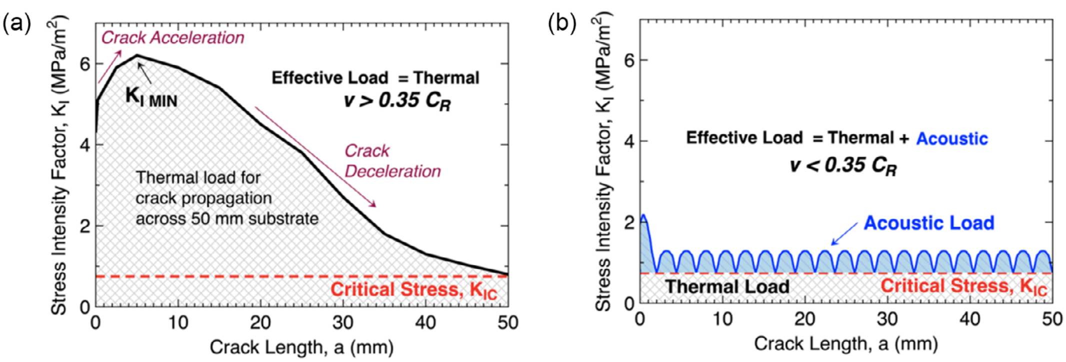

FIGURE 2 | a) Representation of the stress intensity relative to crack propagation through a sample in spontaneous spalling, with the maximum stress intensity required to spontaneously spall the entirety of a 2" wafer. The total stress (area under the solid line) is quite high. Arbitrary values are used for the stress intensity. b) Representation of the stress intensity relative to crack propagation while employing the Sonic Lift-off (SLO) technique. The maximum stress intensity required, as well as the total stress to spall a 2" wafer is lower than that in spontaneous spalling. Arbitrary values are used for the stress intensity, but the relative relationship to a) holds. The thermal load refers to the stress input to the system through the coefficient of thermal expansion mismatch between the stressor and the substrate. In spontaneous spalling (a), that thermal load is the only driving force of the spall. Using Sonic Lift-off, the thermal load can be much lower as the additional energy from the ultrasonic modulation adds a driving force for the spall front propagation. In all cases, the crack front velocity (v) must exceed the critical velocity (C_R) of the crack in the material for the spall to propagate.

stress in the system is lower. Different ultrasonic modulations can be used to create a slower crack front.

In addition to lowering the stress of the system, tuning the ultrasonic modulation affects the surface produced by the SLO process. Three modulations were tested that produced progressively slower maximum velocities (V_{max}). The crack velocity directly affects the high frequency features (the faceting of the GaAs substrate) while the low frequency (longer-range thickness variation of the spall) is affected by nonuniformity in the stressor. The visual differences in Figure 4a–c) are largely due to variation in stressor thickness across the wafer and edge effects from the spall interacting with the edge of the wafer. Modulation 1 had a measured V_{max} of 1400 m/s, modulation 2 had a measured V_{max} of 1080 m/s, and modulation 3 had a measured V_{max} of 830 m/s. The surface maps show that in all three modulations, there is a large area of smooth substrate, but as expected, the areas of higher height variation decrease with a decrease in V_{max} (Figure 4d–f). The defect in the middle of the measured substrate of Modulation 2 (Figure 4e) is due to a local variation in the stressor thickness and is unrelated to the modulation conditions. A line profile from the wafer flat to the opposite edge of the spalled area shows a similar trend (Figure 4g). The line profile also shows an area of higher

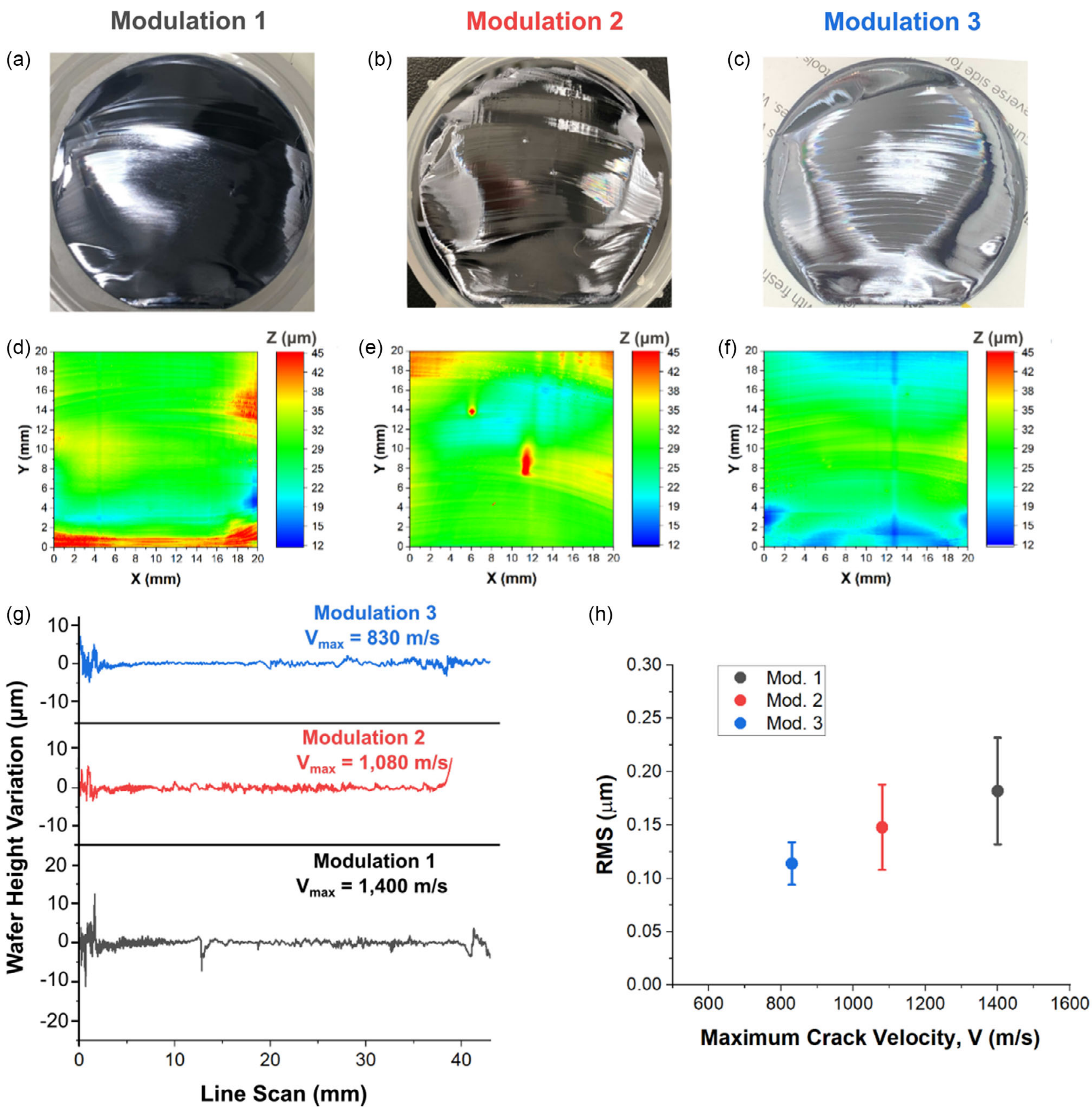

FIGURE 4 | a–c) are top-down photographs of 2” GaAs wafers that have been acoustically spalled under three different ultrasonic modulation conditions. These photographs correspond to the surface maps in d–f). A linear profile from the flat of each wafer to the opposite side of the spalled area is shown in g) as well as the measured V_{max} resulting from each modulation. h) shows an analysis of the RMS roughness across the wafer with the bars representing a standard deviation.

roughness near the flat, where the spall was initiated, which is due to the higher initial stress used to initiate the crack front and aligns with the mechanism of the SLO process described above. An analysis of the high-frequency RMS roughness, as determined from the line scans, shows less roughness and less variation in high-frequency roughness across the wafer as V_{max} decreases (Figure 4h). By altering the ultrasonic modulation in the SLO process, the surface roughness of the resulting substrate surface can be minimized.

3.2 | Device Results

The SLO process was used to exfoliate two different architectures of MOVPE-grown GaAs solar cell devices from their respective GaAs substrates. We demonstrated SLO on 'upright cells' from RIT, where the solar cell layers are deposited in order, from bottom to top, so that the sun-facing side of the device is at the top of the structure after growth, and on 'inverted-growth cells' from NREL, where the structure is grown upside down and then re-oriented during post-growth processing.

While an inverted device structure inherently benefits from the SLO process, as the substrate must be removed regardless, upright devices can also benefit from this technique. Often, the substrate is thinned on upright cells to reduce weight [23]. The SLO process allows for minimal additional substrate to be included with active device layers while also allowing the growth substrate to be reused to grow more upright devices. In addition, the upright structure allows for a simpler processing flow to produce a functional device. If the stressor must be removed, an upright device processing does not require a temporary handle to be used (Figure 1), preventing the need for a double transfer that could lower the yield of final devices. The upright structure also does not require any metallization step prior to spalling (which can interfere with the stressor adhesion), but the stressor layer that is applied to the front surface of the cell needs to be removed following spalling so that it does not parasitically absorb incident light.

Inverted cells, on the other hand, are more complicated because of the additional need to remove the substrate and bond the semiconductor to a permanent handle, but lend themselves more readily to substrate removal techniques and to the incorporation of highly reflective back mirrors that can boost the voltage [24, 25]. For general inverted cells, the back contact is deposited directly on the epitaxial surface layer, the semiconductor is bonded to a handle and the substrate is removed by ELO or etching [26]. For an SLO spalling process, the stressor layer is deposited on the back metal such that the back metal has to be included in the calculation of the spalling stress and may interfere with the spalling process if not compatible. On the other hand, because the stressor is on the back-side of the cell, it does not necessarily have to be removed after spalling. To be compatible with SLO, both types of cells must be transferred to a mechanical handle after exfoliation.

Inverted and upright devices grown on epi-ready wafers were spalled from the wafer using the SLO procedure, resulting in a spall depth of 29 and 34 μm, respectively. Figure 5a,b shows the measured current–voltage characteristics and EQE of the inverted devices as well as corresponding baseline cells that were processed without spalling. The efficiency of the inverted baseline device is 26.51% while the SLO device is 26.80%. Figure 5c,d

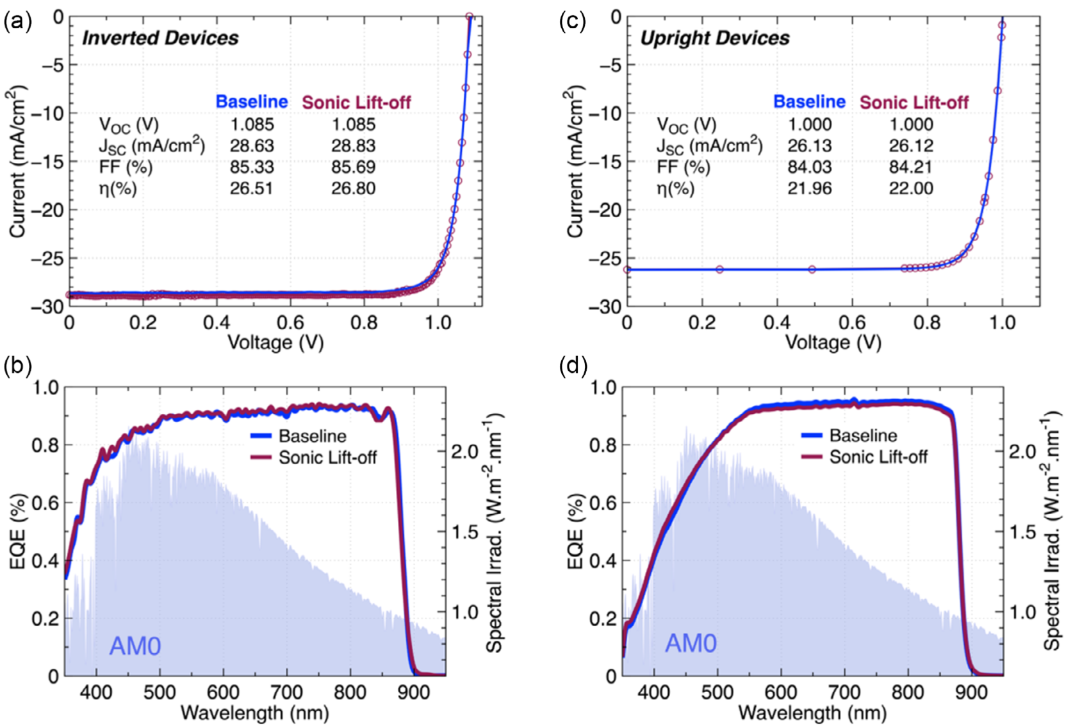

FIGURE 5 | (a) IV curve SLO inverted device compared to cell baseline (taken at AM 1.5G); (b) external quantum efficiency for the SLO inverted device versus the baseline and the AM0 spectra; (c) IV curve SLO upright device compared to cell baseline (taken at AM 1.5G); and (d) external quantum efficiency for the SLO upright device versus the baseline and the AM0 spectra.

shows the same electrical measurements of the upright devices. The efficiency of the upright device shows an baseline efficiency of 21.96% with the SLO device at 22.00%. For both orientations, the spalled devices showed the same performance as the corresponding baseline devices. In addition, the current–voltage (IV) and EQE curves show the same shape with no losses, indicating no degradation caused by the SLO process.

The two cell architectures show slightly different behavior from each other. This is partially due to the growth and processing at two different facilities (RIT and NREL), but there are some structural differences that account for it. The upright cell, grown at RIT, uses an AlInP window layer, and while transparent, the direct growth of the AlInP on GaAs can be problematic. The decreased response of the cell in the short wavelengths and slightly lower V_{OC} indicate that the passivation is slightly poorer for the AlInP window layer than the InGaP/AlInP bilayer window utilized by NREL. This also contributes to a decrease in J_{SC}. In addition, the inverted structure employs a more transparent AlGaAs back contact [24] and a back mirror using the back gold metallization, giving a slight boost to the J_{SC} though increased response in the long wavelengths.

4 | Conclusion

SLO has been shown to have good tunability over spall depth and surface morphology through adjustment of the stressor thickness and ultrasonic modulation. The unique aspect of the ultrasonic modulation allows for a reduced roughness, even when spalling materials that have a faceted cleavage plane such as (100) GaAs. In addition, the electrical characterization of the spalled solar cells shows a solar cell efficiency of 26.5% versus 26.8% (inverted) and 22.0% versus 22.0% (upright) with no significant degradation compared to the baseline.

This work shows a valuable proof-of-concept that exfoliated device layers are not damaged by the SLO process itself, but there are still inherently difficulties present in processing the thin, released layers. Wide-spread adoption of this technology would be limited if yield is affected by a potential double transfer step (as was done in the case of the inverted devices here) or while removing the stressor. More work must be done to evaluate different process flows and the resulting cell yield. It would also be valuable to demonstrate a large-area exfoliated device that is inline with commercial III–V cell structures. In addition, work on regrowth on these substrates has been started [27, 28], but more investigation into the regrowth on spalled surfaces with demonstrations of multiple reuses and resulting cell yields and performances must be performed to prove this technology viable.

Acknowledgements

The authors would like to thank John Mangum for providing the electron channeling contrast imaging shown in the supplementary information. This work was authored in part by Alliance for Sustainable Energy, LLC, the Manager and Operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under contract no. DE-AC36-08GO28308. Funding was provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office under award 08973. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.